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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/997,530
Filing Date: November 30, 2001
Appellant(s): MASTER ET AL.

Wayne L. Tang, Reg. No. 36,028
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/22/2010 appealing from the Office action mailed 9/25/2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 182-305

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

5768561	Wise	6-1998
5794062	Baxter	8-1998
6005943	Cohen et al.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 182-246, 248-276, 278-305 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise U.S. Patent No. 5,768,561 (hereinafter Wise) in view of Baxter U.S. Patent No. 5,794,062 (hereinafter Baxter).

Claim 182:

As per claim 182, Wise teaches a system for adaptive configuration, the system comprising:	Wise, Fig. 137; see also abstract, reconfiguration processing circuits
a first computational unit having a configurable basic architecture	see Wise, Fig. 137, the components at the y inputs (i.e., Y[1,0], Y[5,4], etc) and before the 'the common block' are the first computational unit. Note, the components include adder, subtractor, multiplier etc.
including a first plurality of heterogeneous computational elements	see Wise, Fig. 137, the computational unit at the Y input of fig. 137 includes carry-save multiplier, carry save adder, carry save subtractor. Note these components are heterogeneous computational elements. See also the bottom of Fig. 137 "Key" which shows the name of each component (resolving adder, subtractor, etc)
and a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together	See Wise, Fig. 137, 'the "common block", wherein the first portion of the 'common block' is equivalent to the claimed first interconnection network. The first portion of the 'common block' as shown in Fig. 137 configurably coupling the components at the Y inputs including, adders, subtractors or multipliers which read on applicant's claimed '*coupling the first plurality of heterogeneous computation element together*'
the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function	see Wise, Fig. 137, wherein the first interconnection network (the first portion of the common block as explained above) configures the interconnections between the first plurality of heterogeneous computational elements (the elements at the Y inputs as explained above, i.e., adder, multiplier, subtractor etc) in response to the first configuration information to perform a basic computation function (the first portion of the common block configures the components at the Y input (adder, multiplier, subtractor) to perform a certain function, for instance, the first portion of the common block can be configure to perform either addition or a subtraction which is a basic computation function); see also Fig. 141 which shows the configuration of the common block
a second computational unit having a configurable complex processing architecture	Wise, Fig. 137, the 'd elements' at the x output which includes (d1, d3, d7 and d5). As explained in the 'Key', the d1 shows a carry-save multiplier and a resolving adder/subtractor which is considered to be a complex processing architecture. Note the applicant did not define

	the degree of complexity, so the 'complex processing architecture' is considered to be the architecture of the 'carry save multiplier' or the 'resolving adder/subtractor'. See also, dynamic adaptive configuration, col. 6, line 57 to col. 7, line 12.
including a second plurality of heterogeneous computational elements	See Wise, Fig. 137, (elements at the x output, which includes a carry-save multiplier and a resolving adder/subtractor). Note the multiplier and the adder/subtractor are heterogeneous computational elements. See also x[2,5] of Fig. 37, when reconfigure in a second functional mode which includes, carry save multiplier, carry save subtractor/adder
and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together	See Wise, second portion of 'common block' of Fig. 137 when functioning in a second mode x[2,5]. Note the second portion of the 'common block' is equivalent to the claimed 'second interconnection network'. The second portion of the common block configurable coupling the components of the Y inputs including multipliers, adder/subtractors which reads on applicant's claimed '*coupling the second plurality of heterogeneous computation element together*'
the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function	see Wise, Fig. 137, wherein the second interconnection network (the second portion of the common block as explained above) configures the interconnections between the second plurality of heterogeneous computational elements (the elements at the X inputs as explained above, i.e., multiplier, adder/subtractor etc) in response to the second configuration information to perform a complex computation function (the second portion of the common block configures the components at the X input (multiplier, adder/subtractor) to perform a specific complex function such as carry save multiplier or matrix multiplier. Furthermore, the second portion of the common block can be configure to perform either carry-save multiplier is a complex computation function); see also Fig. 141 which shows the configuration of the common block
With respect to the first limitation "*a memory adapted to store configuration information including a first configuration information and a second information*", Wise did not specifically show a memory adapted to store first configuration information and second configuration. However, the secondary reference, Baxter taught a memory for storing first configuration information and a second configuration information (see Baxter, Fig. 3a for the reconfiguration information, as shown in the figure, there are multiple reconfiguration	

information; see col. 5, lines 61-67, wherein more than one reconfiguration information is stored in memory; see also col. 5, lines 28-37, lines 48-60 and Fig. 4 for the implementation of the reconfiguration information). It would have been obvious to one of ordinary skill in the relevant art at the time of the invention was made to use Baxter in the invention of Wise of having a memory for storing the first configuration and a second configuration as claimed for the purpose of providing Wise's invention the ability to reuse the configuration information as stored in a memory, thereby increasing the adaptability of the system, and because Wise also taught a memory map for mapping hardware resources into the memory address (see Wise, col. 259, lines 10-25), and that his multiplexed network (see interconnection common box in Fig. 137) showed the points at which needed to be stored (see Wise, col. 262, lines 14-20), which was a suggestion of the desirability to save the configuration information, such as the connection points, into a memory, and for doing so, provided a motivation. Wise also showed the storage of the configuration information (see Wise, the RAM organized into common control block in col. 265, lines 43-53; see also the common control block of Fig. 137)

3. As per claim 183, Wise further teaches the system of claim 182, wherein the configuration information provides a first system operating mode of the plurality of operating modes (see Wise, Fig. 137, operating in either carry-save multiplier, carry save adder or a carry save subtractor).

4. As per claim 184, Wise further teaches the system of claim 182, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information (see Wise, col. 64, lines 34-50, 'request').

5. As per claim 185, Wise further teaches the system of claim 182, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information (see functional mode of x[3,4] of Fig. 137, note, accessing the memory or read/write to

memory is considered to be a memory function; see also col. 95, lines 35-41, read/write from memory).

6. As per claim 186, Wise further teaches the system of claim 182, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface (see Wise, microprocessor read port in col. 260, lines 32-35; see also RAM in col. 265, lines 43-53).

7. As per claim 187, Wise further teaches the system of claim 182, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits (see Wise, Discrete cosine transform in col. 4, lines 1-11 for background; see also the data packets in col. 13, lines 53-57).

8. As per claim 188, Examiner holds that integrated circuit was already well known in the art at the time of the invention was made, thus the system shown in Wise must be embodied in an integrated circuit (see also Wise abstract, reconfiguration processing circuit).

9. As per claims 189-190, Baxter further teaches wherein the computational units are organized in a configurable computing matrix and the computing matrix is coupled to a matrix interconnection network, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing

matrix having a plurality of computational units (see Baxter, the interconnect Matrix in Fig. 1, see also the interconnect matrix for selectively routing in col. 10, lines 15-38). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use Baxter in Wise's invention for including the selectively routing the first and second configuration information as claimed because the use of Baxter would provide Wise the capability to reconfigure the processing elements at a predefined set of selection, thereby increasing the flexibility of the configurations, and because Wise also taught his interconnection network (see the common box in 137 with a multiplexed circuit, see Wise, col. 262, lines 14-19), which was a suggestion of the applicability of the selective routing, and for the above reasons, provided a motivation.

10. As per claims 191-193, Baxter further teaches wherein a first configured function of the configurable computing matrix is as a controller, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices, wherein the controller is a RISC controller (see Baxter, Fig. 1, S machines, T machines, I/O T machines and I/O devices; see also col. 10, lines 26-38).

11. As per claim 194, Wise further teaches the system of claim 182, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the

transmission of data and configuration information (see Wise, Fig. 137, interconnection network and col. 4, lines 21-23).

12. As per claim 195, Baxter further teaches system of claim 194, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions (see Baxter, col. 10, lines 26-38).

13. As per claim 196, Wise further teaches the system of claim 182, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

14. As per claim 197, Wise further teaches the system of claim 182, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28).

15. As per claim 198, Wise further teaches the system of claim 182, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the second plurality of

heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

16. As per claim 199, Wise further teaches the system of claim 198, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

17. As per claim 200, Wise further teaches the system of claim 199, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

18. As per claim 201, Wise further teaches the system of claim 197, wherein the basic computational function is a logic function; and wherein the complex processing function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

19. As per claim 202, Wise further teaches the system of claim 196, wherein the first computational unit operates at a bit level; and wherein the second computational unit

operates at a word level (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

20. As per claim 203, Wise further teaches the system of claim 202, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

21. As per claim 204, Wise further teaches the system of claim 182, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions (see Wise, Fig. 137, adder, multiplier; col. 4, lines 8-9, and col. 30, line 62 to col. 31, line 4).

22. As per claim 205, Wise further teaches the system of claim 204, wherein the basic computational function is a logic function; and wherein the complex processing

function is a digital signal processing function (see Wise, col. 4, lines 8-9 and the transforms; see also col. 30, lines 62-67).

23. As per claim 206, Wise further teaches the system of claim 205, wherein the basic computational function comprises bit level manipulation; and wherein the complex processing function comprises word level manipulation (see Wise, col. 40, lines 15-28 and col. 30, line 62 to col. 31, line 4).

24. As per claim 207, Wise further teaches the system of claim 206, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register (see Wise, Fig. 137, for adder, multiplier, subtract and I/O; see also col. 6, line 57 to col. 7, line 12).

25. As per claim 208, Wise further teaches the system of claim 207, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift (see Wise, Fig. 137, for adder, multiplier, subtract and col. 6, line 57 to col. 7, line 12).

26. As per claim 209, Wise further teaches the system of claim 182, further comprising a third interconnection network coupled to the first computational unit and the second computational unit, the third interconnection network sending the configuration information to the computational units (see Wise, Fig. 137 and col. 262, lines 14-42).

27. As per claim 210, Wise further teaches the system of claim 209, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network (see Wise, Fig. 137 and col. 262, lines 14-42, this would be based on the configuration, wherein the first network can be a denser than the second network, it would have been an obvious matter of design choice).

28. As per claim 211, Wise further teaches the system of claim 182, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements (see Fig. 137, multiplexers, such as the multiplexers in the output of the adders or the multiplier at the Y input).

29. As per claim 212, Wise further teaches the system of claim 211, wherein the configuration information includes control signals to control the multiplexers (see Wise, Fig. 137 and col. 262, lines 14-42).

30. As per claim 213, it's rejected for the same reasons set forth above in claim 182.

31. As per claims 214-221, they are rejected for the same reasons set forth above in the corresponding claims 183-190.

32. As per claim 222, the features of claim 222 are similar to the limitations of claim 182; therefore claim 222 is rejected for the same reasons set forth above in claim 182.

33. As per claims 223-244, they are rejected for the same reasons set forth above in the corresponding claims 191-212.

34. As per claim 245, the system of claim 213, wherein the first interconnection network provides a third configuration information to reconfigure the first configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information (As explained above in claim 182, Baxter shows a memory for storing configuration including multiple configuration information as shown in Baxter, Fig. 3a and col. 5, lines 61-67; Fig. 3a shows first, second and third configuration information which is stored in memory as explained in

col. 5, lines 28-37 and lines 48-60. The motivation utilized in the combination of claim 182, super, applies equally as well to claim 245).

35. As per claim 246, the method of claim 246 is performed by the processor of claim 182. Consequently, claim 246 is rejected for the same reaons set forth in the rejection of claim 182 above.

36. As per claims 248, 249, 250, 251, they are rejected for the same reasons set forth above in the corresponding claims 183, 186, 189, 190.

37. As per claim 252, the features of claim 252 are similar to the limitations of claim 182; therefore claim 252 is rejected for the same reasons set forth above in claim 182.

38. As per claims 253-274, they are rejected for the same reasons set forth above in the corresponding claims 191-212.

39. As per claim 275, it is rejected for the same reasons set forth above in claim 245.

40. As per claim 276, the method of claim 276 is performed by the processor of claim 182. Consequently, claim 276 is rejected for the same reaons set forth in the rejection of claim 182 above. Note, the configuration interconnections of a first and second plurailty for hetergenous computational elemetns are similar to claim 182. Also, the configuration

information received and transmitted is stored in memory similar to claim 182. Therefore, claim 276 is a method claim performed by the processor of claim 182 and thus rejected for the same reasonsing set forth above in claim 182.

41. As per claims 278, 279, 280, 281, they are rejected for the same reasons set forth above in the corresponding claims 183, 186, 189, 190.

42. As per claim 282, it is rejected for the same reasons set forth above in claim 245.

43. As per claims 283-304, they are rejected for the same reasons set forth above in the corresponding claims 191-212.

44. As per claim 305, it is rejected for the same reasons set forth above in claim 245.

45. Claim 247 and 277 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise in view of Baxter, as applied to claims above, and further in view of Cohen et al. U.S. Patent No. 6,005,943 (hereinafter Cohen).

46. As to claim 247, neither Wise nor Baxter specifically showed the authorization to receive the configuration as claimed. However, Cohen taught authorization of the configuration (see Cohen, Fig. 1, step 7, see also Fig. 2, col. 5, lines 5-52 for 'authorization'). It would have been obvious to one of ordinary skill in the art to use

Cohen in Wise for including the authorization of the configuration as claimed because the use of Cohen would provide Wise the ability to accept the configuration information based on a predetermined set of requirements and restrictions, therefore increasing system security in Wise.

47. As per claim 277, it's rejected for the same reasons set forth above in claim 247.

(10) Response to Argument

At page 11-12 of the brief, appellant argues:

"*The main cited references, Wise and Baxter, are both prior art systems of types that the specification discusses and dismisses. Wise is generally directed toward a hardware implemented video decompression circuit. (Ex. C, Abstract). Although Wise makes reference to "reconfiguration," such reconfiguration is not performed using an interconnection network to change interconnections between different computational elements as required by the present claims. Instead the reconfiguration references specific functions that are achieved in the integrated circuit and selected via instructions from tokens. However, new instructions that are not part of the instruction set could not reconfigure the connections between the elements in the circuit on Wise to perform new functions. Wise is more of the nature of an ASIC that has limited functions and cannot be reconfigured to perform new, unplanned functions*"

This argument is not persuasive because as explained in the rejection above, Wise shows a reconfiguration interconnection network as shown in Fig. 137 that reconfigures specific functions (i.e., adders, subtractors or multipliers). The appellant argues that Wise 'reconfiguration' is not the same as the claimed 'reconfiguration'. The examiner would like to point out that the rejection is based on the broadest reasonable interpretation of the claim language along with explicit and unambiguous definitions of

the claim terminology which must be made available in the specification. The instant application clearly fails to provide a specific or an explicit definition for the term 'reconfiguration', therefore, the term 'reconfiguration' is interpreted in it's plain meaning as well known in the art. Wise clearly shows a reconfiguration system that configures certain elements to perform a specific function such as add, multiple, subtract etc. The reconfiguration as claimed is used to reconfigure the system to perform specific functions as explained by appellant in page 9 of the brief "*Another distinct feature is the use of different or heterogeneous computation elements such as adders, multipliers, functional generators...",* however, this explanation of by applicant's specification is similar to Wise reference wherein the system is reconfigured to either add, subtract or multiply. Note Wise also uses the term 'reconfiguration' which is also what the claims recite as well. Furthermore, see Wise col. 12, lines 45-47 "*Reconfigurable process stage (RPS): A stage, which in response to a recognized token, reconfigures itself to perform various operations"* This shows that the "reconfiguration system" as taught by Wise reconfigures itself to perform various functions.

Appellant also argues "*However, new instructions that are not part of the instruction set could not reconfigure the connections between the elements in the circuit on Wise to perform new Functions",* This argument is not persuasive because these features upon which applicant relies (i.e., *new instructions that are not part of the instruction set could not reconfigure the connections between the elements in the circuit)* are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See

In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the argued 'unplanned functions' are not recited in the rejected claims.

At page 12, appellant argues:

"*The Final Office Action has cited the inverse discrete cosine transform (IDCT) block shown in Fig. 137 of Wise as disclosing a first computational units having computational elements such as the carry-save multiplier, carry save adder and carry save subtractor. (Ex. B, p.3). The Final Office Action has characterized Fig. 137 as disclosing a first interconnection network that configures interconnections between the blocks citing Col. 262, 11. 14-42 of Wise. (Ex. B, p. 3). This section is actually is a summary of various components in Fig. 137 but does not disclose an interconnection network allowing changing connections between the different components in Fig. 137.*"

The examiner respectfully disagrees because as explained in the rejection above, the "common block" of Fig. 137 has multiple lines to reconfigure the circuit to perform a specific function such as addition, subtraction or multiplication. This is also admitted by appellant in the first argument "*Instead the reconfiguration references specific functions that are achieved in the integrated circuit and selected via instructions from tokens"* This admission by appellant shows that the system of Wise can be reconfigure to perform any specific function. See also Wise col. 12, lines 45-47 "*Reconfigurable process stage (RPS): A stage, which in response to a recognized token, reconfigures itself to perform various operations"* This shows that the "reconfiguration system" as taught by Wise reconfigures itself to perform various functions.

At page 12-13, appellant argues:

"*The overall architecture in Fig. 137 makes it clear that there is no interconnection network since none of the connections shown between the various adders, subtractors and multipliers may be changed. The IDCT block in Fig. 137 may perform only a single function related to the cosine transform and cannot be configured. Finally, Fig. 137 does not describe two computational units, it is at best a single computational unit that performs a singular function.*"

The examiner respectfully disagrees. It's not clear from appellant's arguments why Wise system connections need to be changed? All it is required from the claim is an 'interconnection network' to configure heterogeneous elements. Wise Fig. 137 shows a reconfiguration system that reconfigures different elements such as adders, subtractors or multipliers. With respect to appellant arguments that "*Fig. 137 does not describe two computational units, it is at best a single computation unit that performs a singular function",* this argument is not persuasive because as clearly shown in Fig. 137 of Wise, there a column of computation elements (first computational unit as claimed) at the Y input before the 'common block' and there is another column of computation elements (second computational unit as claimed) at the X output after the 'common clock'. Each of the computation elements (first and second) as shown in Fig. 137 have different components, including adders, subtractors, multipliers, adders/subtractors etc.

At page 13, appellant argues:

"*Baxter generally relates to a repeated array of S-machines and T-machines that are connected by a matrix with corresponding input devices. (Ex. D, Col. 4, 11.55-65). Baxter is typical of known FPGA art that required massive interconnection infrastructure in the FPGAs that make up the dynamically reconfigurable processing unit (DRPU) 32 of the S-Machine 12 and the FPGA that makes up the T-Machines 18. (Ex. D, Col. 5, 11. 14-16, Col. 6, 11.8-19, Col. 10, 11.46-59). The Final Office Action has cited Fig. 3A and 4 of Baxter as disclosing a memory for storing first and second configuration information. (Ex. B, p. 4). As noted above, the memory 34 of a given S-machine*

includes complex configuration instructions necessary for an FPGA which makes up the DRPU 32. (Ex. D, Col. 11, 11.38-47). Baxter makes clear that the configuration is used for an FPGA which is composed of homogeneous (identical) computational elements and therefore is significantly different from the present claims. (Ex. D, Col. 15, 11.34-66)."

The examiner respectfully disagrees because as explained above in the rejection, Baxter was introduced to show a memory to store configuration information (see Baxter, Fig. 3a which shows different configuration information (i.e., ISA 1, ISA 2, etc), see also col. 5, lines 61-67 and col. 5, lines 28-37 which shows the memory storing different configuration information). Note, with respect to the underlined argument above, Baxter clear shows different configuration as shown in Fig. 3a (ISA 1, ISA 2, ISA 0 etc) and col. 12, lines 31-42 which explicitly recites "*In the present invention, each s-machine's DRPU 32 can be rapidly runtime-configured to directly implement multiple ISAs through the use of unique configure data set for each desired ISA.....namely, ISA 1, 2, 3, 4, and K",* Note 'ISA' stands for 'instruction set architecture', therefore, there are multiple instruction set architecture configurations stored in the memory.

At page 13-14, Appellant argues:

"*Claims 183,213,246 and 276 require a first computational unit having a configurable basic architecture and a second computational unit having a configurable complex processing architecture. The Final Office Action has cited Fig. 137 of Wise as disclosing for both of these units. (Ex. B, p. 3). The block shown in Fig. 137 is a single computational unit and cannot be separated into two computational units each performing separate functions and therefore does not anticipate these claim elements. The Final Office Action has cited Col 6, ll. 57-67 and Col. 7, ll. 1-12 of Wise for complex multiplication and the x [2,5] output of Fig. 137 as showing a second functional mode. (Ex. B, p. 3). Applicant respectfully submits that this is an incorrect reading of Wise. Col. 6, 1.57 to Col. 7, 1. 12 generally describes the different functions along various processing stages but does not disclose how the processing stages are configured via*

the tokens. (Ex. C). As explained above, the "configuration" refers to predetermined alternate functions which do not use configuration information to change the interconnections between the computational elements such as multipliers and adders in Fig. 137."

The examiner respectfully disagrees because as explained above in the rejection and above arguments, Wise Fig. 137 show a column of computation elements (first computational unit as claimed) at the Y input before the 'common block' and another column of computation elements (second computational unit as claimed) at the X output after the 'common clock'. Each of the computation elements (first and second) as shown in Fig. 137 have different components, including adders, subtractors, multipliers, adders/subtractors etc which reads on the current claim language. Note, applicant's claim language did indicate that the first and second computational units are different and distinct from each other, therefore one computational unit can read on both because the claims are given their broad reasonable interpretation. Nevertheless, assuming that applicant's claim have two different computational units, Wise still reads on the claim language because the first column of computational elements of Fig. 137 (the adders, multiplier before the 'common block') are considered to be the first computational unit and the second column after the 'common block' is the second computational unit (which includes adders/subtractors and multipliers). Note each elements, for instance, an adder computes a different function (i.e., addition) from a multiplier (i.e., multiply). Therefore, each column as explained above can compute different and distinct function.

At page 14, appellant argues:

"Therefore Wise does not disclose a second discrete computational unit since the architecture in Fig. 137 is simply reused for a second round of four inputs rather than a circuit that performs all eight transforms simultaneously as in Fig. 136. Wise does not disclose a first and second computational unit and therefore does not anticipate the claims."

This argument is not persuasive because as detailed in the rejection and argument responses above, Wise teaches all these argued elements. Wise Fig. 137 show a column of computation elements (first computational unit as claimed) at the Y input before the 'common block' and another column of computation elements (second computational unit as claimed) at the X output after the 'common clock'. Each of the computation elements (first and second) as shown in Fig. 137 have different components, including adders, subtractors, multipliers, adders/subtractors etc which reads on the current claim language. Note, applicant's claim language did indicate that the first and second computational units are different and distinct from each other, therefore one computational unit can read on both because the claims are given their broad reasonable interpretation. Nevertheless, assuming that applicant's claim have two different computational units, Wise still reads on the claim language because the first column of computational elements of Fig. 137 (the adders and multiplier before the 'common block') are considered to be the first computational unit and the second column after the 'common block' is the second computational unit (which includes adders/subtractors and multipliers). Note each elements, for instance, an adder

computes a different function (i.e., addition) from a multiplier (i.e., multiply). Therefore, each column as explained above can compute different and distinct function.

At page 15, appellant argues:

"*The Office Action therefore is misconstruing operation of the circuit in Fig. 137. The IDCT in Fig. 137 is not two separate computational units since the entirety of the circuit performs a four value transformation twice. (Ex. C). Further, it is not "reconfigured" to perform a second function, the same function is simply performed twice ("reused") with different values to achieve the desired result of eight total cosine transformations. (Ex. C, Col. 262, 1.29). Since Fig. 137 and the remainder of Wise does not disclose two reconfigurable computational units, the claims are not anticipated by Wise or the combination of Wise with Baxter.*"

This argument is not persuasive because as detailed in the rejection and argument responses above, Wise teaches all these argued elements. Specifically, see the previous two responses which clearly explain the argued two computational units.

At page 16, section 4, appellant argues:

"All of the independent claims require interconnection networks for each computational unit that each "configurably couple the respective plurality of computational elements" and for "configuring interconnections between" the computational elements in response to the configuration information. The Final Office Action has cited Fig. 137 of Wise as disclosing such an interconnection network. However, the Final Office Action has not provided any explanation of what elements in Fig. 137 constitute an interconnection network, let alone a network that may configure the interconnections between the computational elements. An examination of Fig. 137 shows that the connections between the various adders, multipliers and subtractors are permanent wired connections and therefore the connections cannot be changed. Further the connections are more akin to a bus rather than a true network that may route data between each computational element. Even if certain routing may be performed via latches, the set of connections is fixed and data may only be routed to certain computational elements. The configuration in Fig. 137 therefore is not a network because it cannot configure the interconnections between the computational elements.

Since Wise does not disclose an interconnection network, let alone one which changes the interconnections between the computational elements, Wise does not anticipate the pending claims."

This argument is not persuasive because as explained in the rejection and argument responses above, Wise teaches all these argued elements and functions. Furthermore, it's not clear from appellant's arguments why Wise system connections need to be changed? All it is required from the claim is an 'interconnection network' to configure heterogeneous elements. Wise Fig. 137 shows a reconfiguration system that reconfigures different elements such as adders, subtractors or multipliers. Furthermore, see Wise col. 12, lines 45-47 "*Reconfigurable process stage (RPS): A stage, which in response to a recognized token, reconfigures itself to perform various operations"* This shows that the "reconfiguration system" as taught by Wise reconfigures itself to perform various functions.

Also, Wise Fig. 137, the first portion of the 'common block' is equivalent to the claimed first interconnection network. The first portion of the 'common block' configurably coupling the components at the Y inputs including adders, subtractors, or multipliers which read on applicant's claimed "*coupling the first plurality of heterogeneous computation element together*". The wires or interconnection of Wise does not have to be changed but they are reconfigured to either perform a multiplier function or adder function or other specific functions. Furthermore, the applicant claim language uses the term 'reconfiguration' and 'configuration' while the reference (Wise) uses the same terminology 'reconfiguration and also configuration', see Wise i.e., abstract.

With respect to the argument in page 16, section B. Appellant indicated that claims 247 and 277 were improperly rejection but did not provide explanation or arguments on how the features of claims 247 and 277 are not cited by the references. No explanation of why or how the prior art is defective is given. No specific contention of why the examiner's position is flawed or deficient is made. Therefore, the examiner directs applicant's attention to the explanation of the rejections and argument responses above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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